

FIG.1

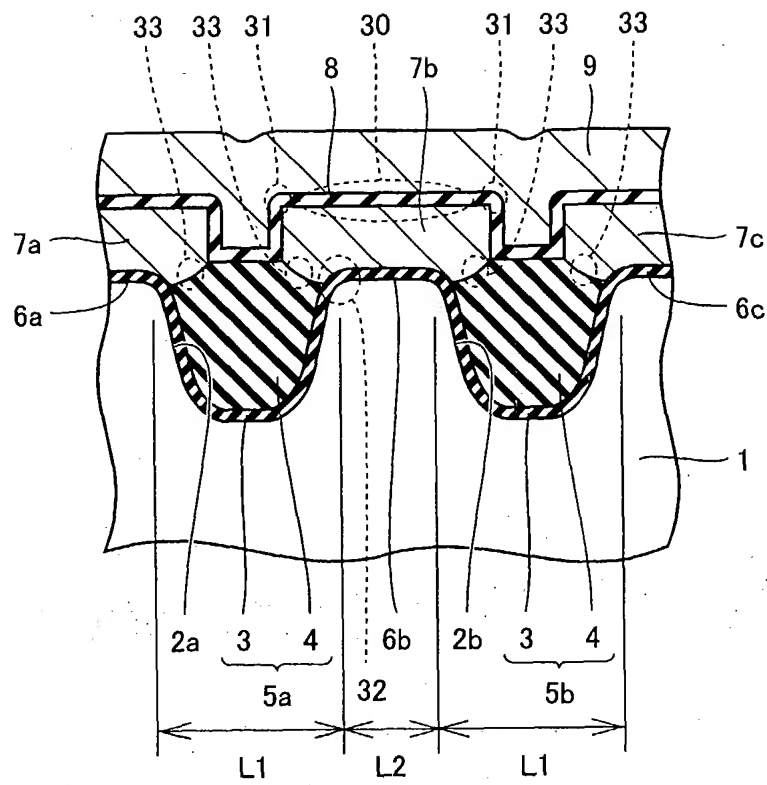


FIG.2

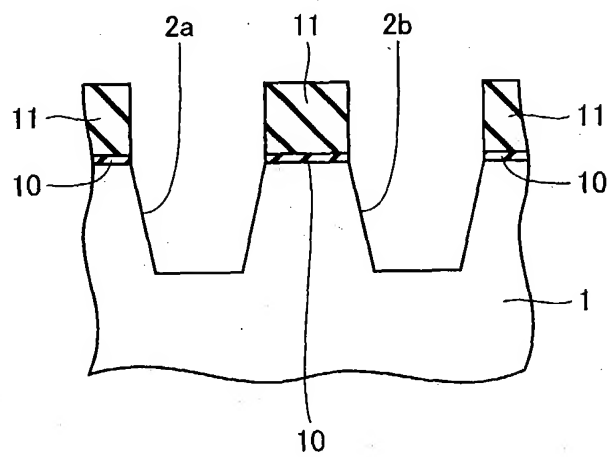


FIG.3

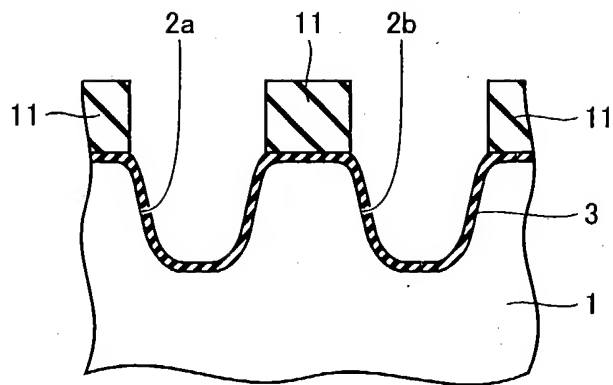


FIG.4

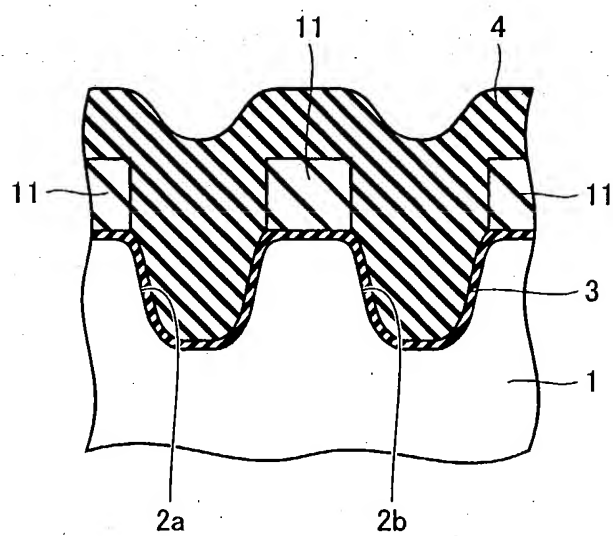


FIG.5

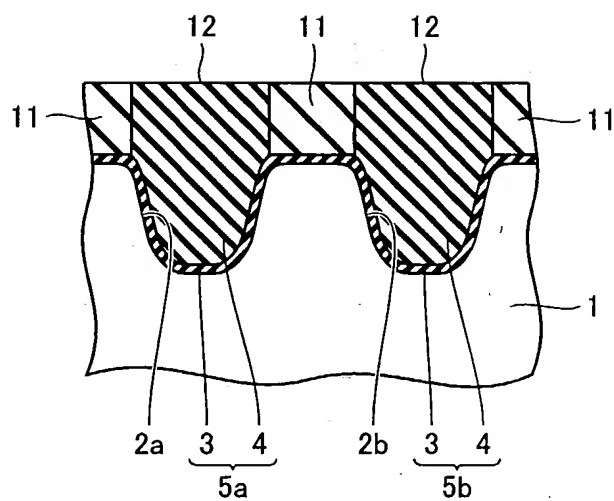


FIG.6

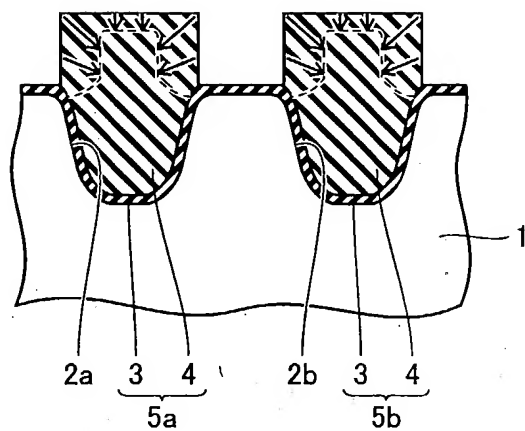


FIG.7

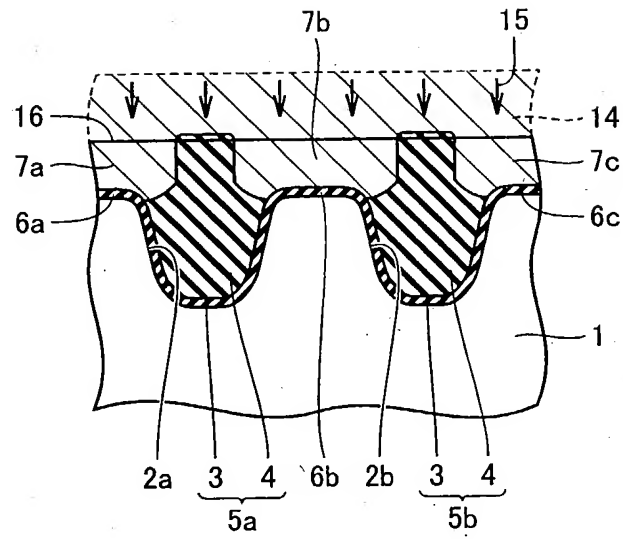


FIG.8

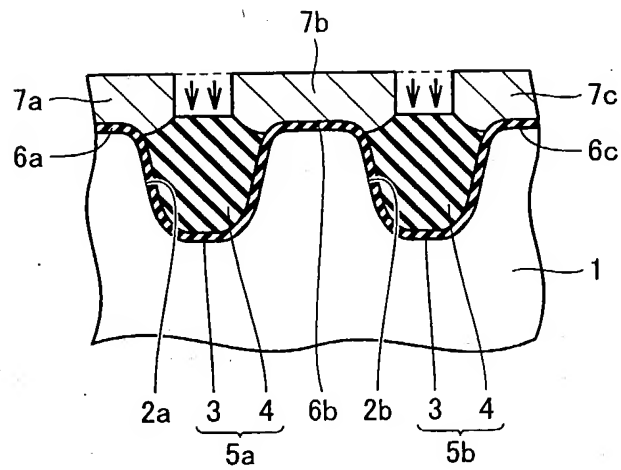


FIG.9

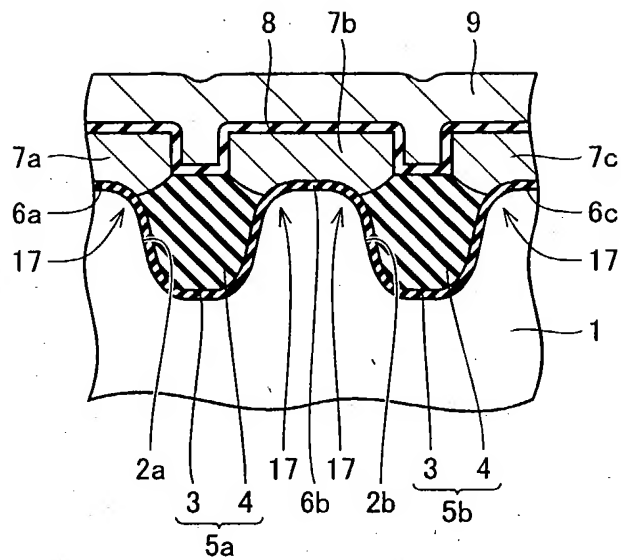


FIG.10

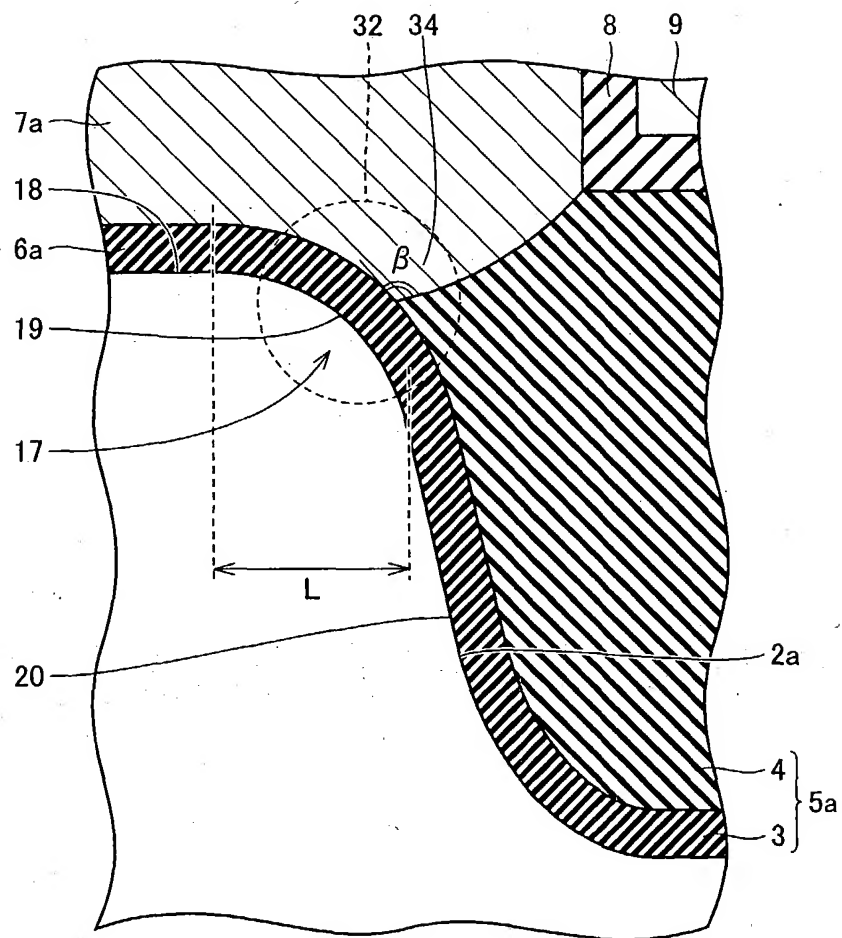


FIG.11

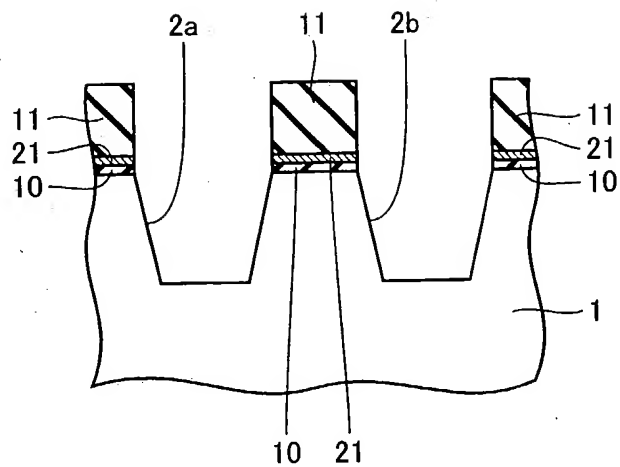


FIG.12

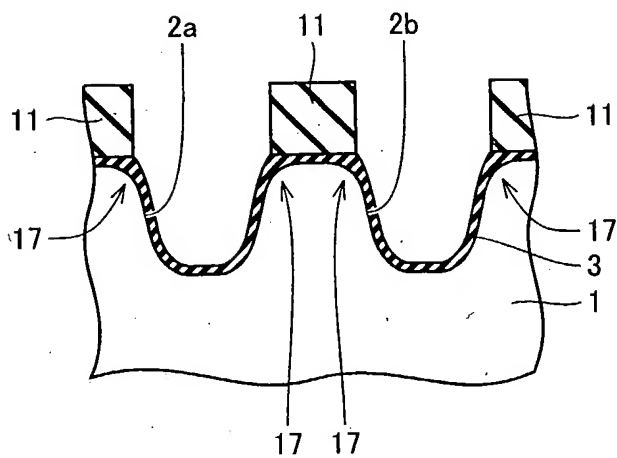


FIG.13

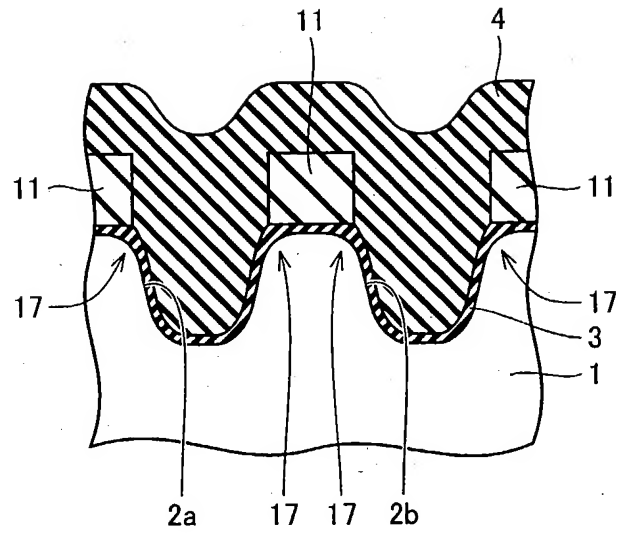


FIG.14

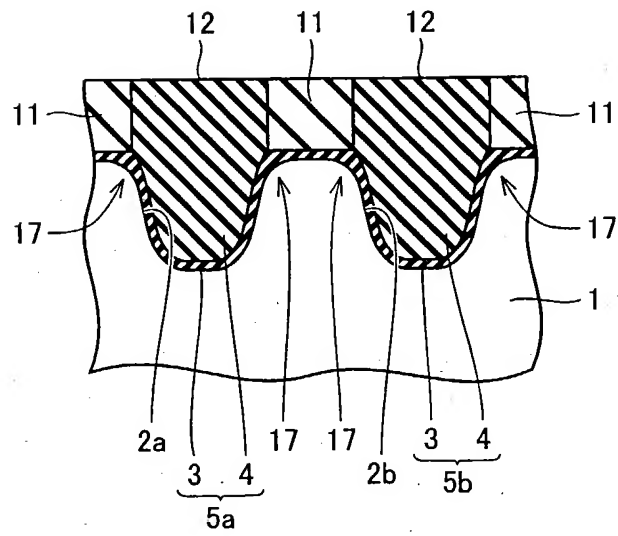


FIG.15

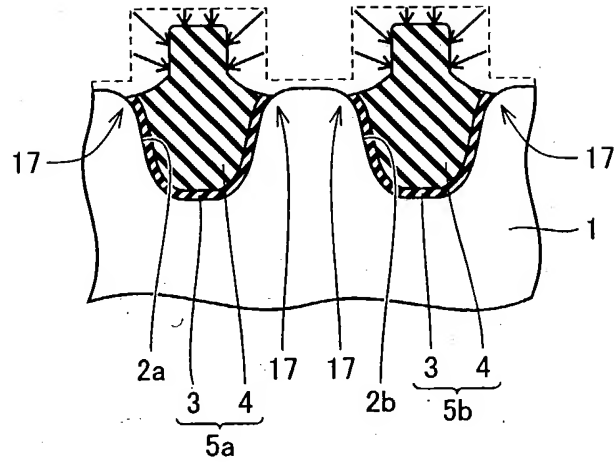


FIG.16

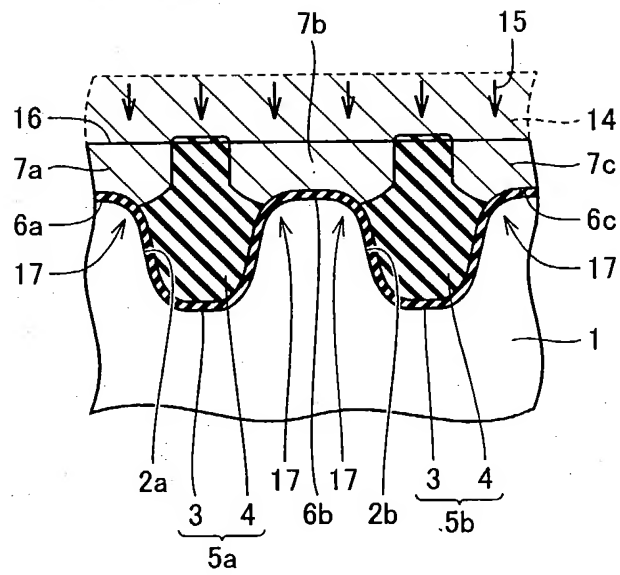


FIG.17

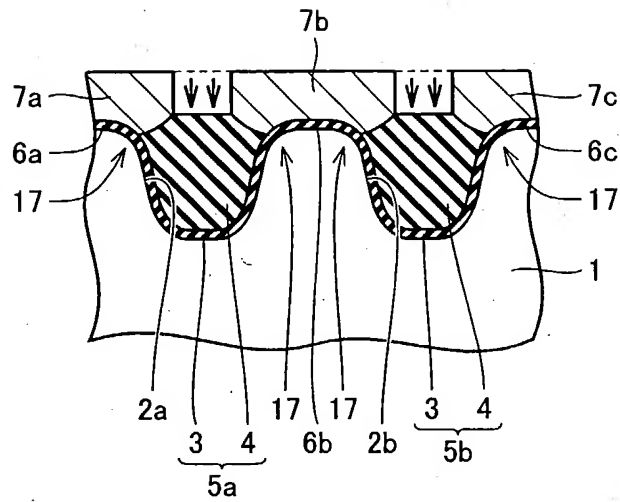


FIG.18

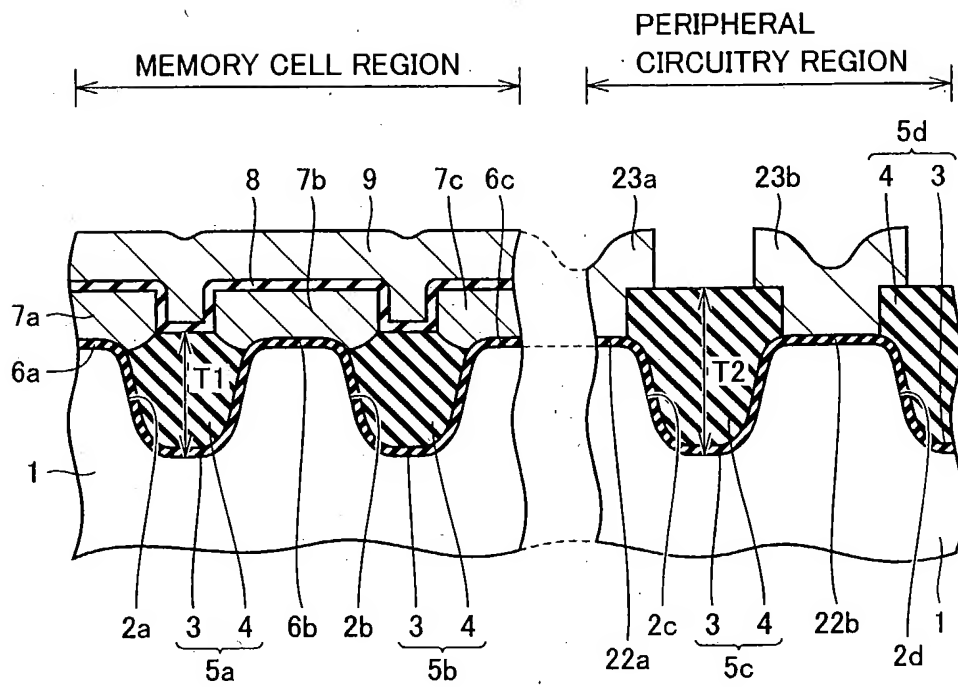


FIG.19

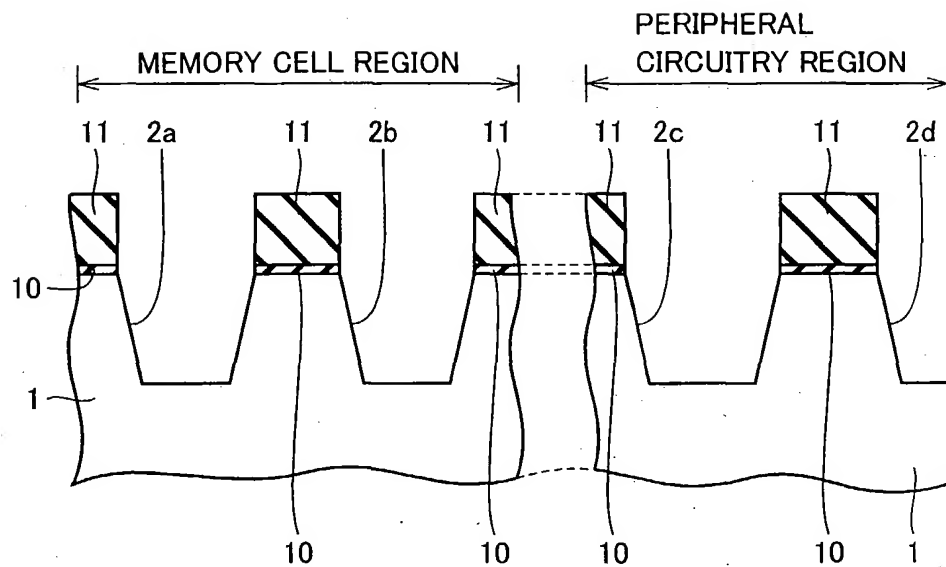


FIG.20

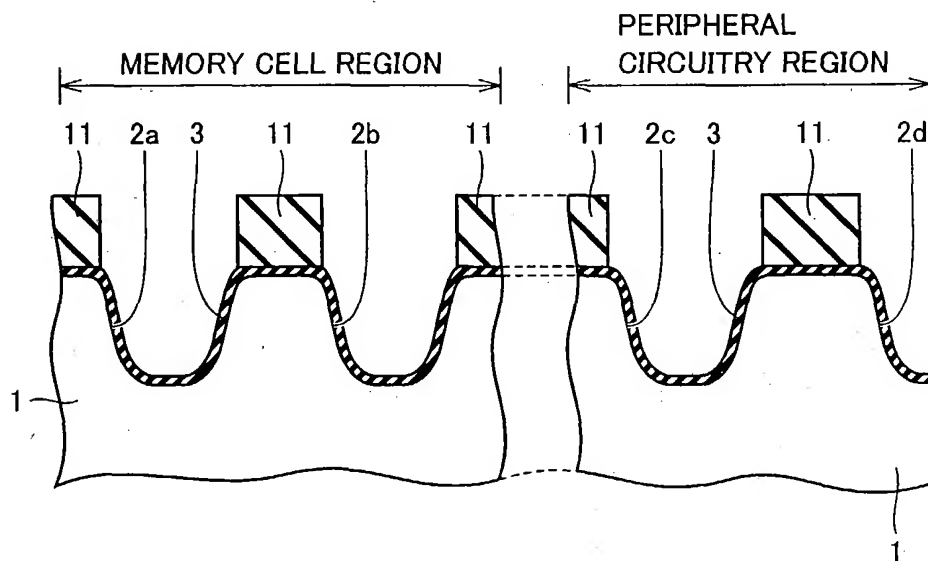


FIG.21

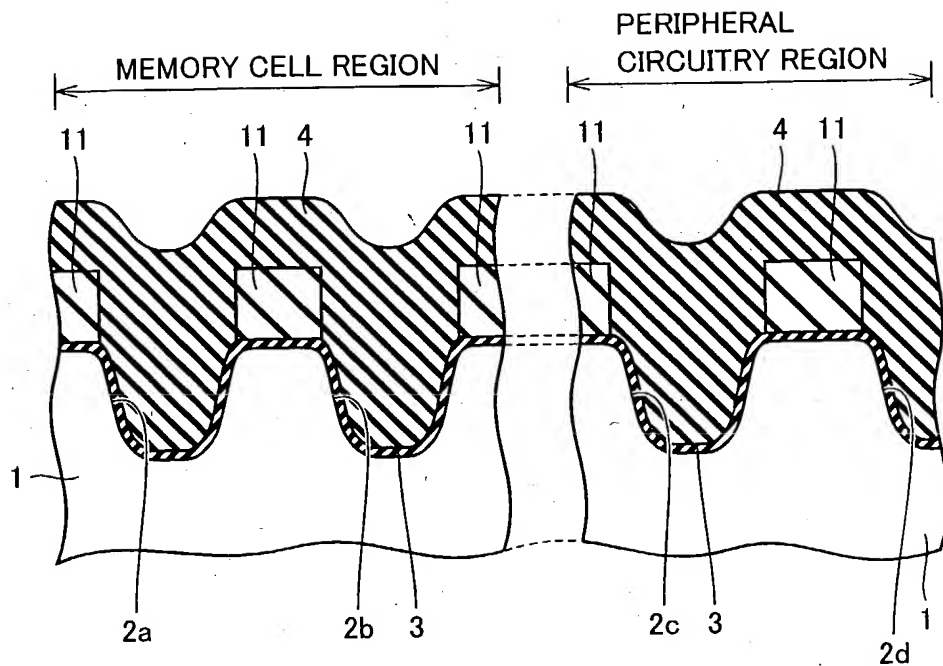


FIG.22

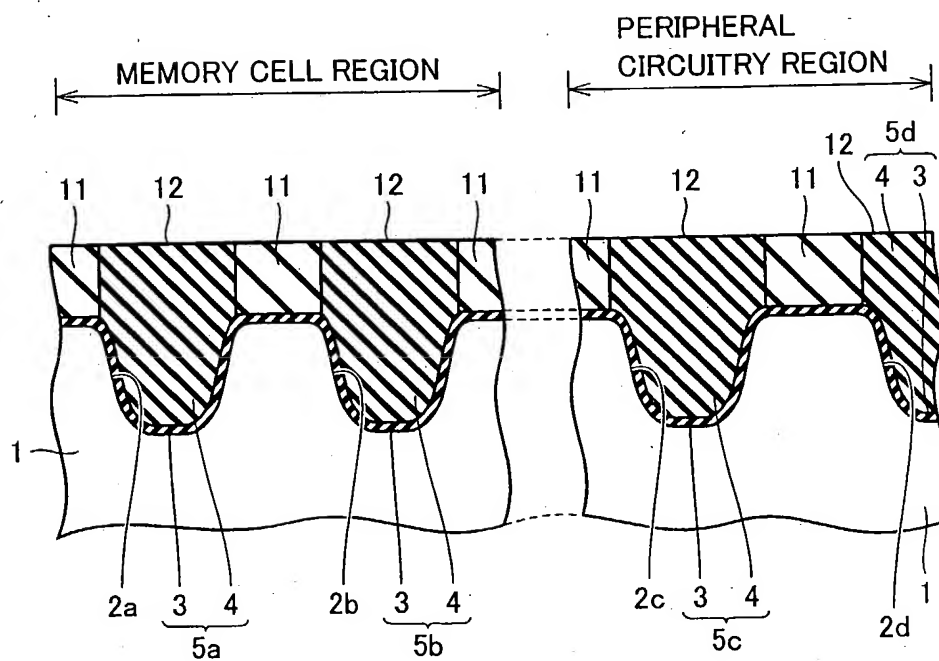


FIG.23

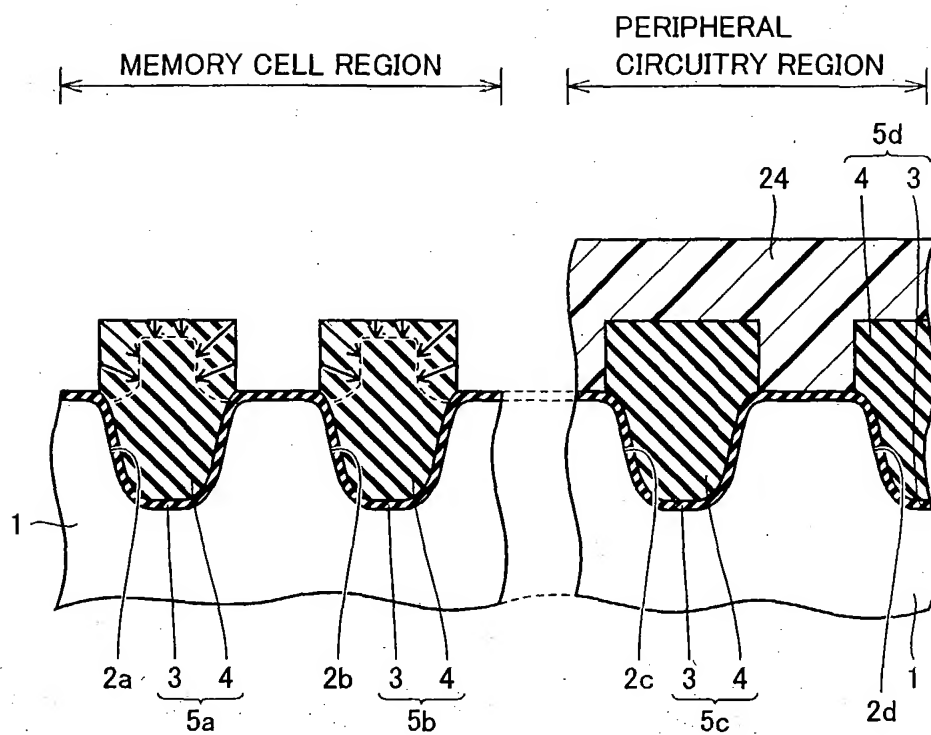
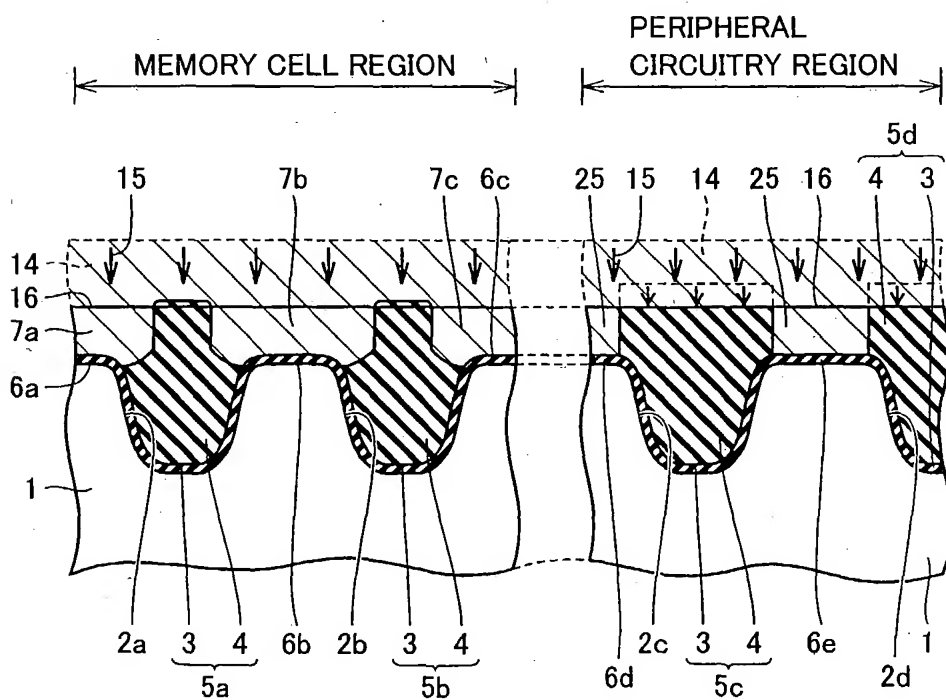


FIG.24



The diagram illustrates a cross-sectional view of a semiconductor device, divided into two main functional areas: the MEMORY CELL REGION and the PERIPHERIAL CIRCUITRY REGION.

MEMORY CELL REGION: This region contains two memory cells. Each cell consists of a substrate (1) with a series of gates (2a, 2b) and a central channel (3). The gates are separated by spacers (4). The top surface is covered by a layer (6a, 6b) and a protective layer (7a, 7b). Arrows indicate the direction of current flow through the channel (3).

PERIPHERIAL CIRCUITRY REGION: This region contains peripheral circuitry. It features a substrate (1) with a series of gates (2c, 2d) and a central channel (3). The gates are separated by spacers (4). The top surface is covered by a layer (6c, 6d) and a protective layer (7c, 7d). Arrows indicate the direction of current flow through the channel (3).

The diagram uses various hatching patterns to distinguish different materials or layers: diagonal lines for the substrate (1), horizontal lines for the gates (2), vertical lines for the spacers (4), and a combination of horizontal and vertical lines for the top layers (6 and 7).

The diagram illustrates a cross-sectional view of a semiconductor device, divided into two main functional areas: the MEMORY CELL REGION and the PERIPHERIAL CIRCUITRY REGION.

MEMORY CELL REGION: This region contains three repeating memory cell structures. Each structure consists of a central gate stack (8) flanked by side gates (7b and 7c). The gate stack is connected to a word line (6c). The side gates are connected to bit lines (2a, 2b, 2c). The bit lines are connected to data lines (3, 4). The data lines are connected to a common data line (5a, 5b, 5c). The memory cell region is separated from the peripheral circuitry region by a dashed line.

PERIPHERIAL CIRCUITRY REGION: This region contains peripheral circuitry structures. Each structure consists of a central gate stack (8) flanked by side gates (7b and 7c). The gate stack is connected to a word line (6c). The side gates are connected to bit lines (2a, 2b, 2c). The bit lines are connected to data lines (3, 4). The data lines are connected to a common data line (5a, 5b, 5c). The peripheral circuitry region is separated from the memory cell region by a dashed line.

Labels and Components:

- 8:** Gate stack
- 7b, 7c:** Side gates
- 6c:** Word line
- 2a, 2b, 2c:** Bit lines
- 3, 4:** Data lines
- 5a, 5b, 5c:** Common data line
- 25:** Peripheral circuitry structure
- 4, 3:** Peripheral circuitry data lines
- 5d:** Peripheral circuitry common data line
- 1:** Substrate
- 6a:** Memory cell region boundary
- 7a:** Peripheral circuitry region boundary

The diagram illustrates a cross-sectional view of a semiconductor device, divided into two main functional areas: the MEMORY CELL REGION and the PERIPHERAL CIRCUITRY REGION.

MEMORY CELL REGION: This region contains three memory cells. Each cell is formed by a series of stacked layers: a bottom layer (1), a first conductive layer (2a, 2b, 2c), a second conductive layer (3), a third conductive layer (4), a fourth conductive layer (5a, 5b, 5c), a fifth conductive layer (6a, 6b, 6c), a sixth conductive layer (7a, 7b, 7c), and a top layer (8). The cells are separated by a central channel (6b) and side channels (6a, 6c). The top layer (8) is patterned to form word lines (7a, 7b, 7c) over the cells.

PERIPHERAL CIRCUITRY REGION: This region contains two peripheral circuit elements. Each element is formed by a series of stacked layers: a bottom layer (1), a first conductive layer (2d, 2e), a second conductive layer (3), a third conductive layer (4), a fourth conductive layer (5d, 5e), a fifth conductive layer (6d, 6e), a sixth conductive layer (7d, 7e), and a top layer (8). The elements are separated by a central channel (6f) and side channels (6g, 6h). The top layer (8) is patterned to form word lines (7d, 7e) over the elements.

The diagram illustrates a cross-sectional view of a semiconductor device, divided into two main functional areas: the MEMORY CELL REGION and the PERIPHERAL CIRCUITRY REGION.

MEMORY CELL REGION: This region contains two memory cells. Each cell consists of a substrate (1) with a series of gates (2a, 2b) and a central channel region (3). The gates are separated by spacers (4). The channel region is covered by a layer (5a, 5b) and is surrounded by a dielectric layer (6a, 6b). The top surface is covered by a layer (7a, 7b) and a passivation layer (8, 9). The peripheral circuitry region is separated from the memory cell region by a dashed line.

PERIPHERAL CIRCUITRY REGION: This region contains peripheral circuitry. It features a substrate (1) with gates (22a, 22b) and a central channel region (3). The gates are separated by spacers (4). The channel region is covered by a layer (5c) and is surrounded by a dielectric layer (6c). The top surface is covered by a layer (7c) and a passivation layer (9). The peripheral circuitry region is separated from the memory cell region by a dashed line.

Labels 1 through 9 identify various components and layers across the device structure.

FIG.29

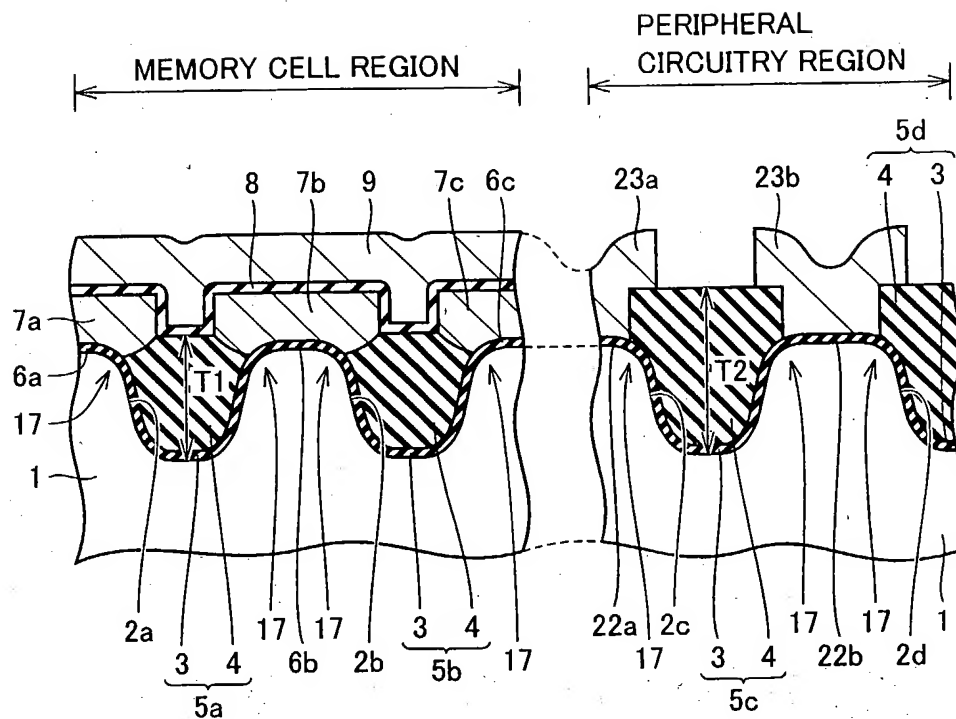


FIG.30

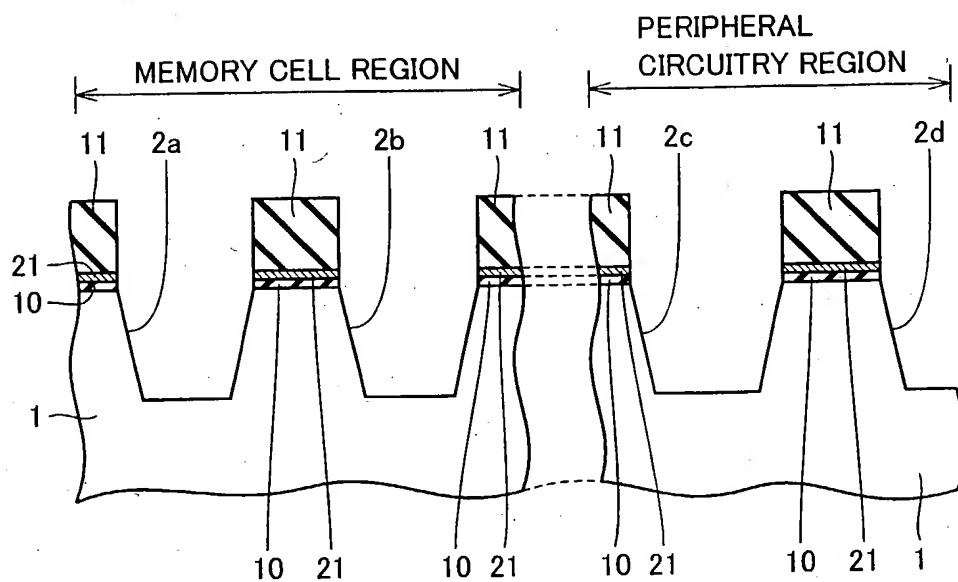


FIG.31

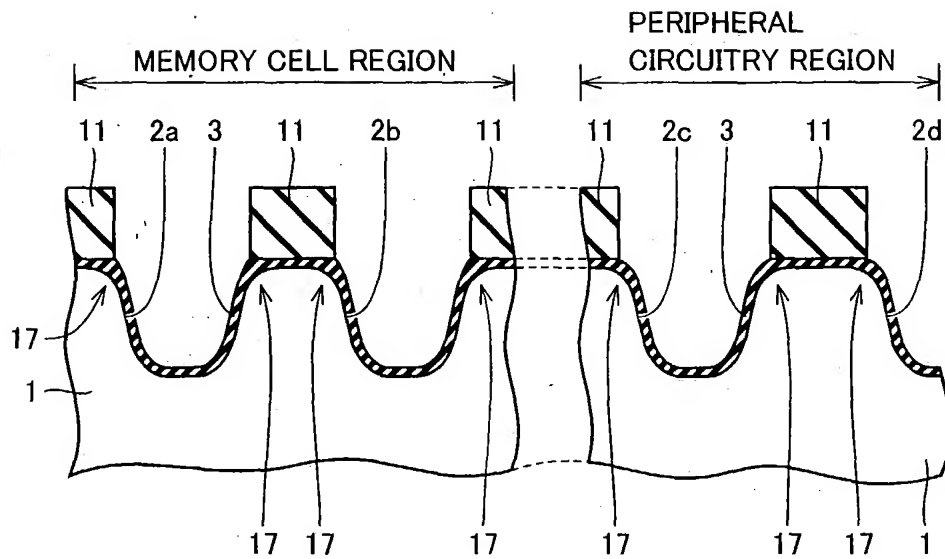


FIG.32

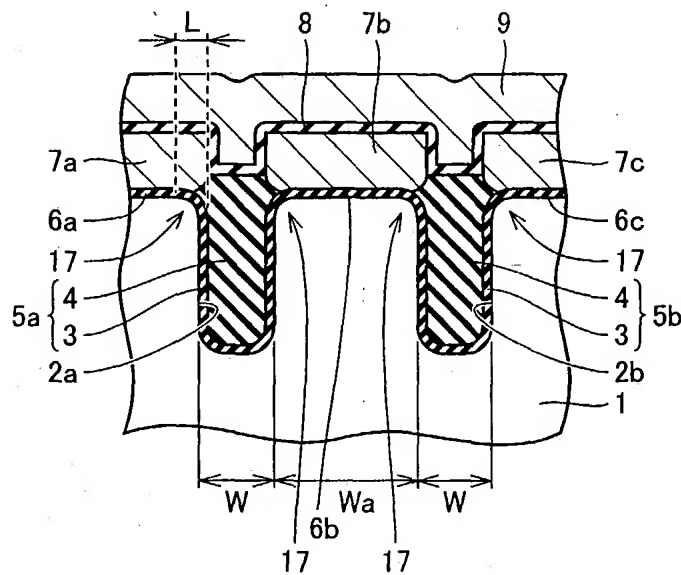


FIG.33

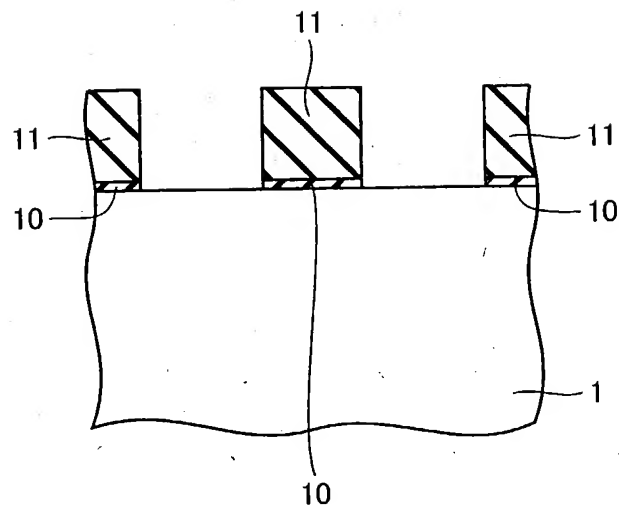


FIG.34

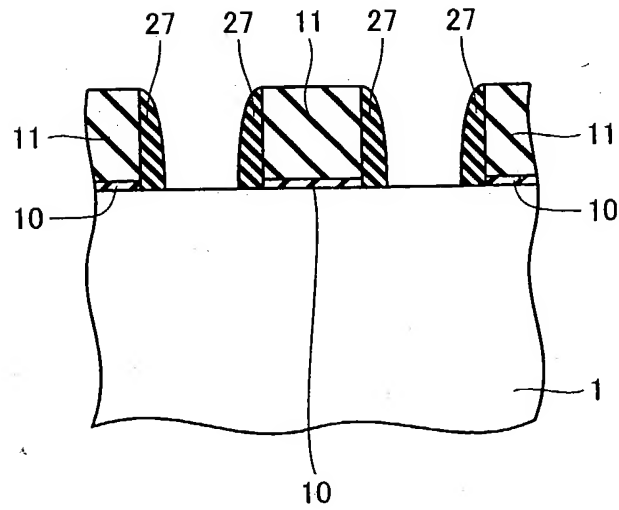


FIG.35

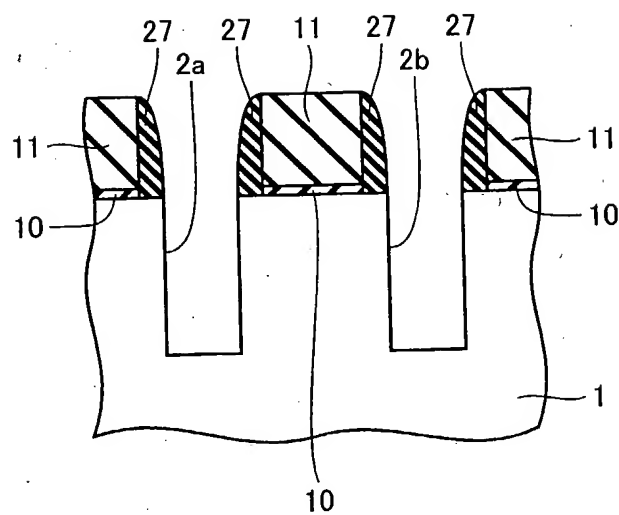


FIG.36

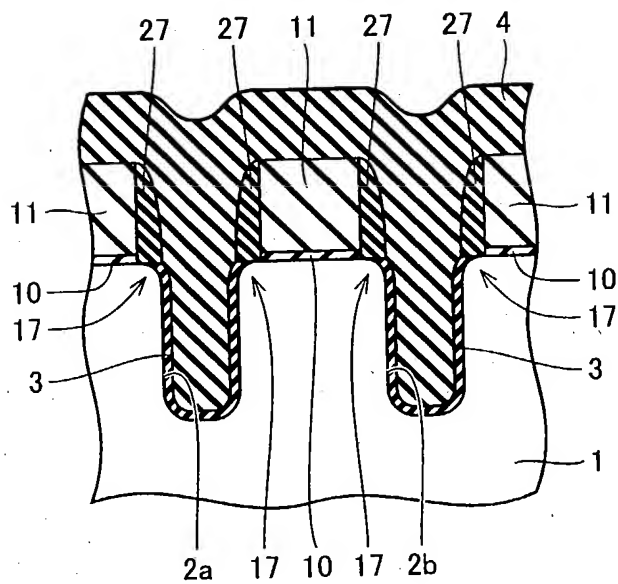


FIG.37

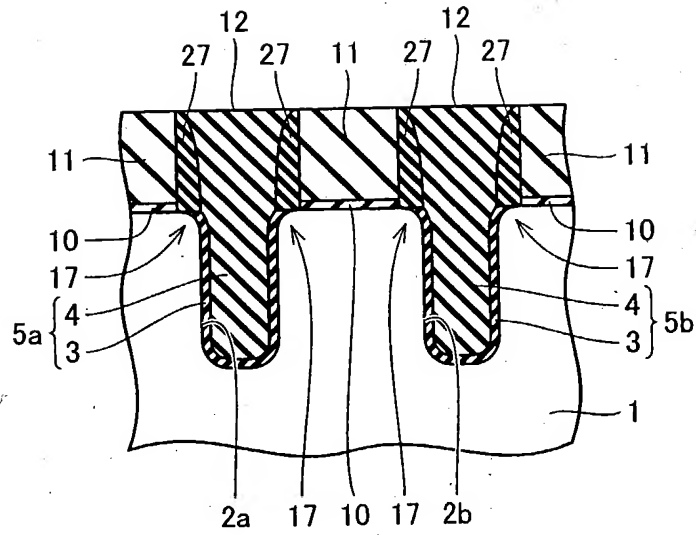


FIG.38

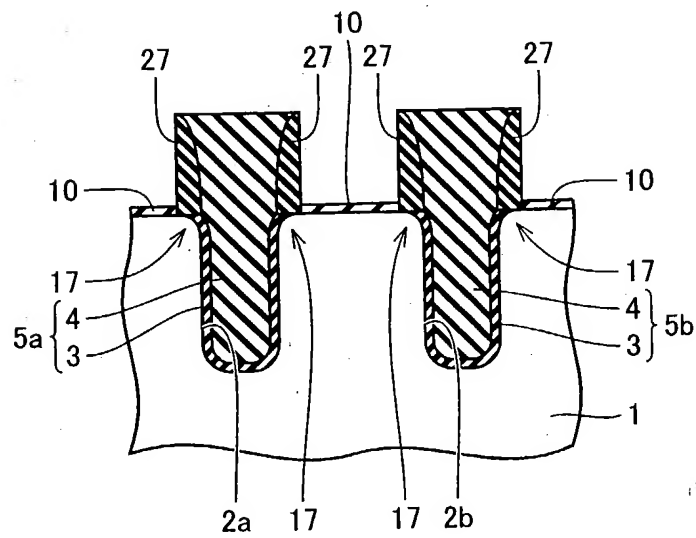


FIG.39

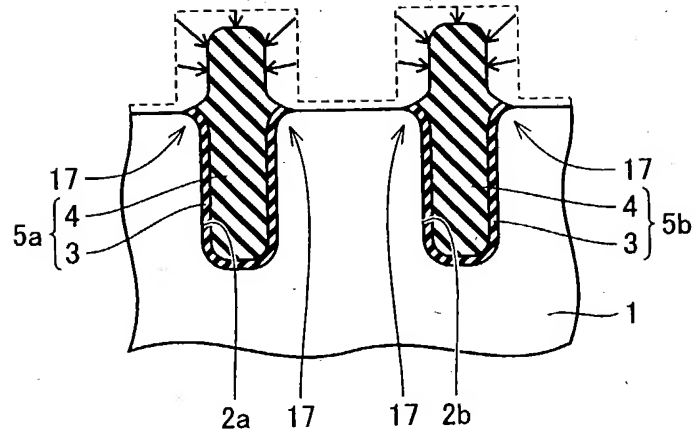


FIG.40

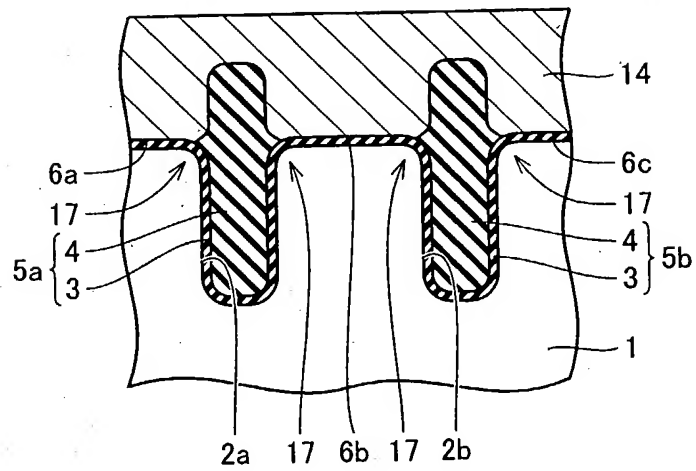


FIG.41

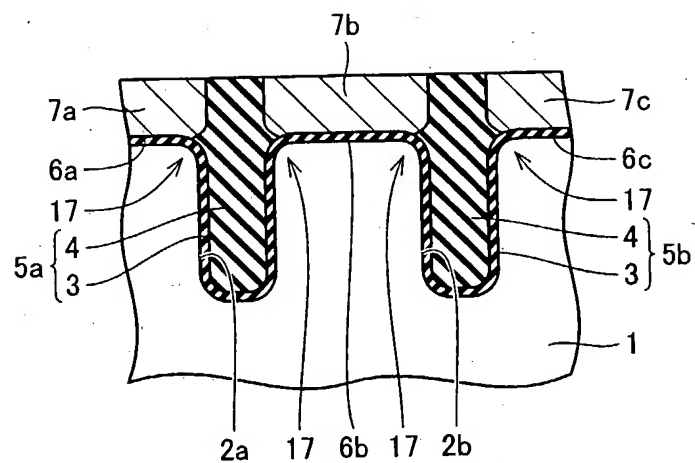


FIG.42

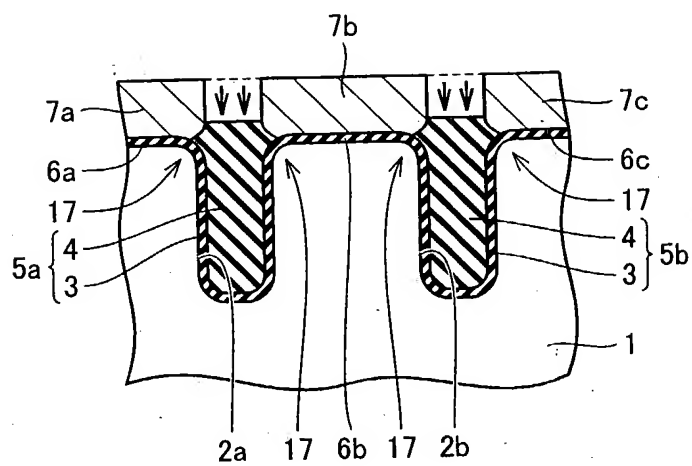


FIG.43

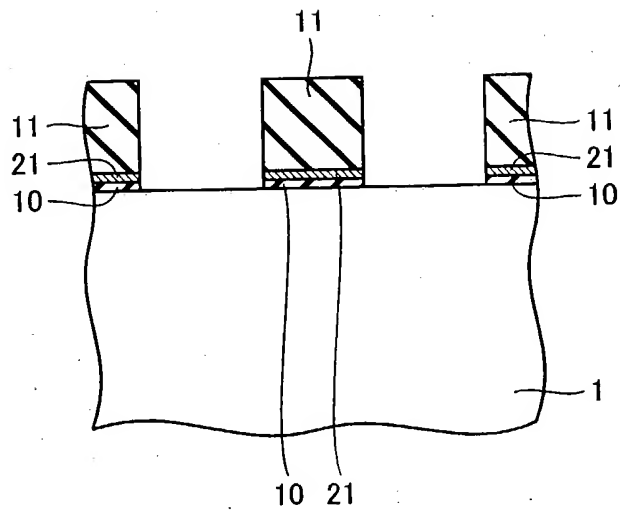


FIG.44

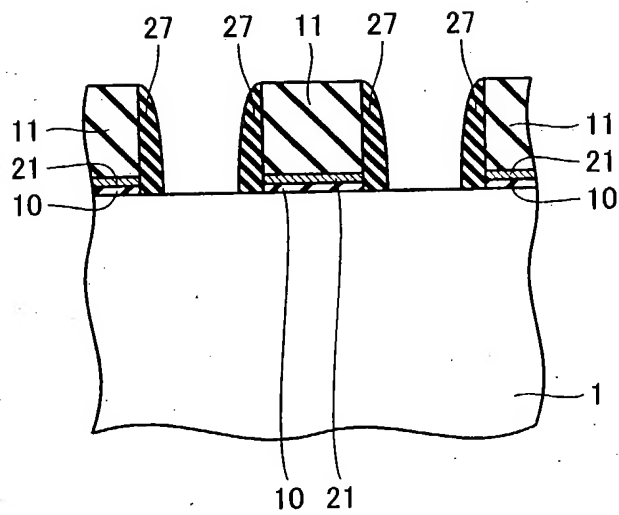


FIG.45

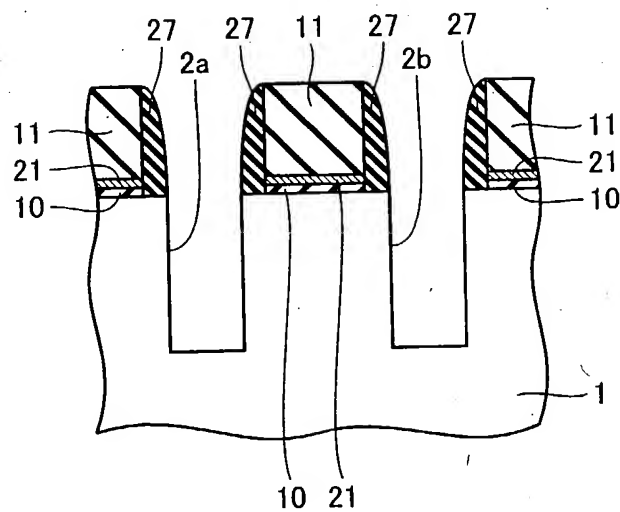


FIG.46

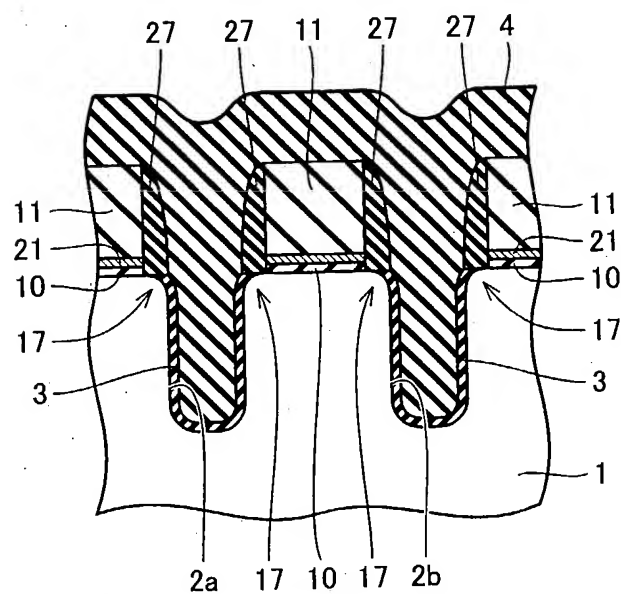


FIG.47

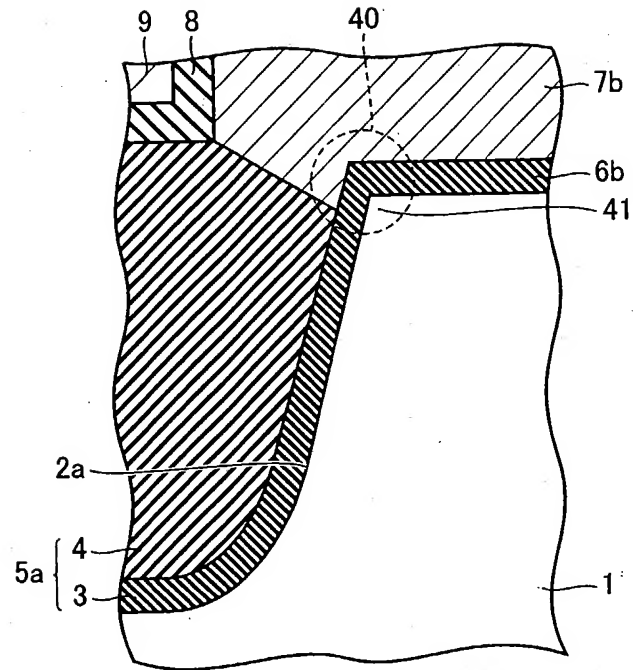


FIG.48

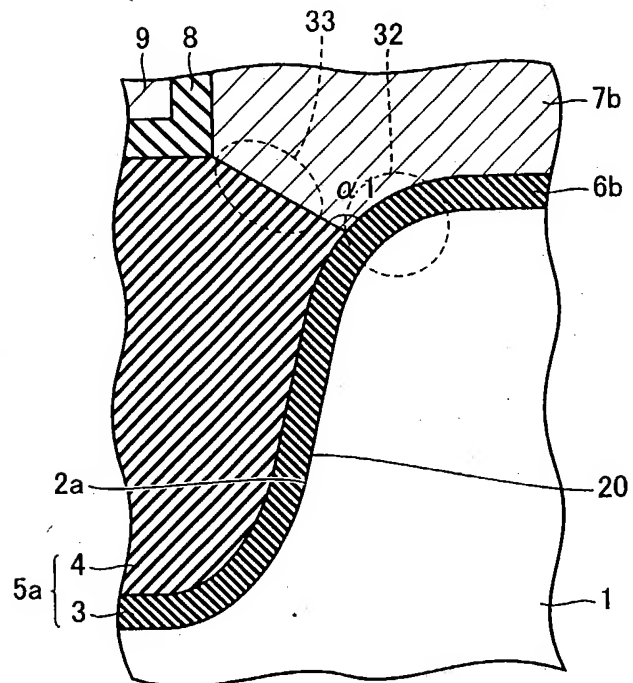


FIG.49

